FIG. 1

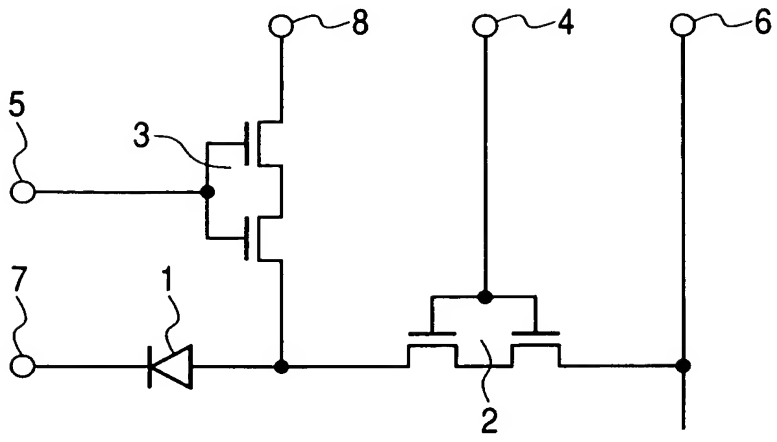

FIG. 2

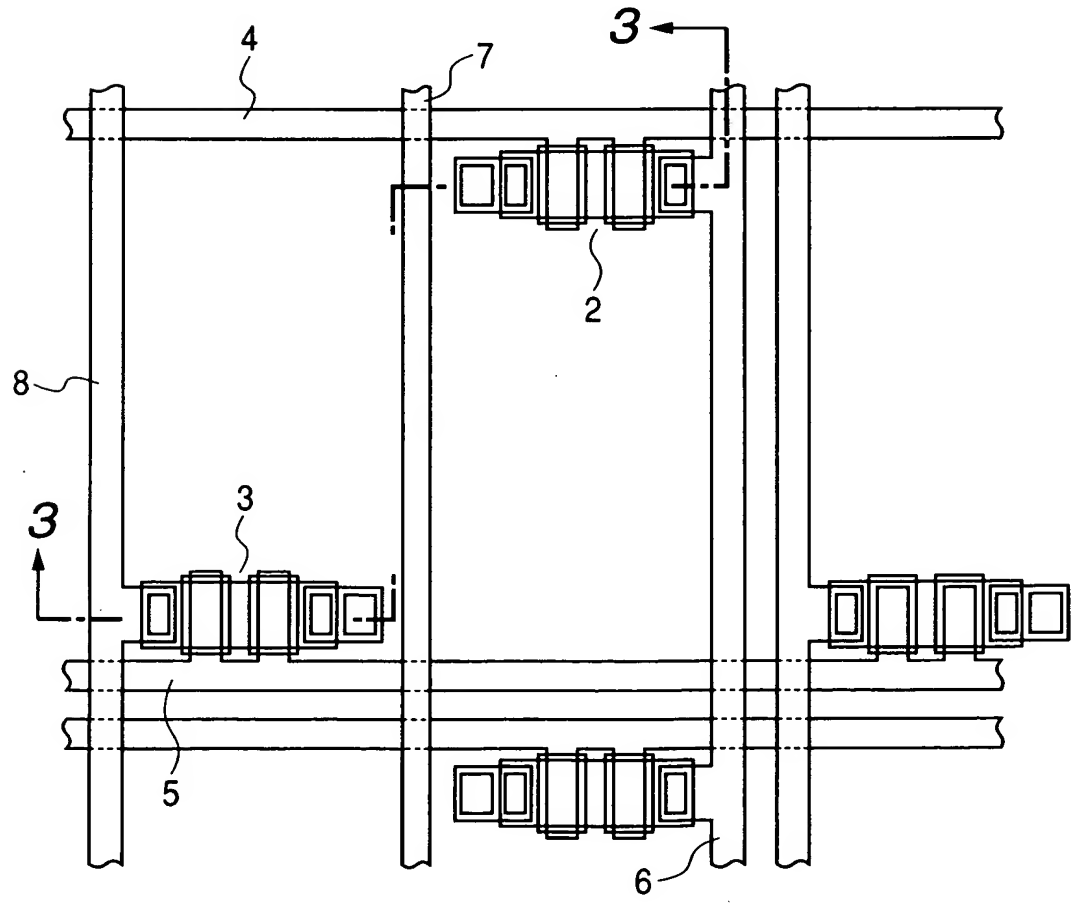

FIG. 3

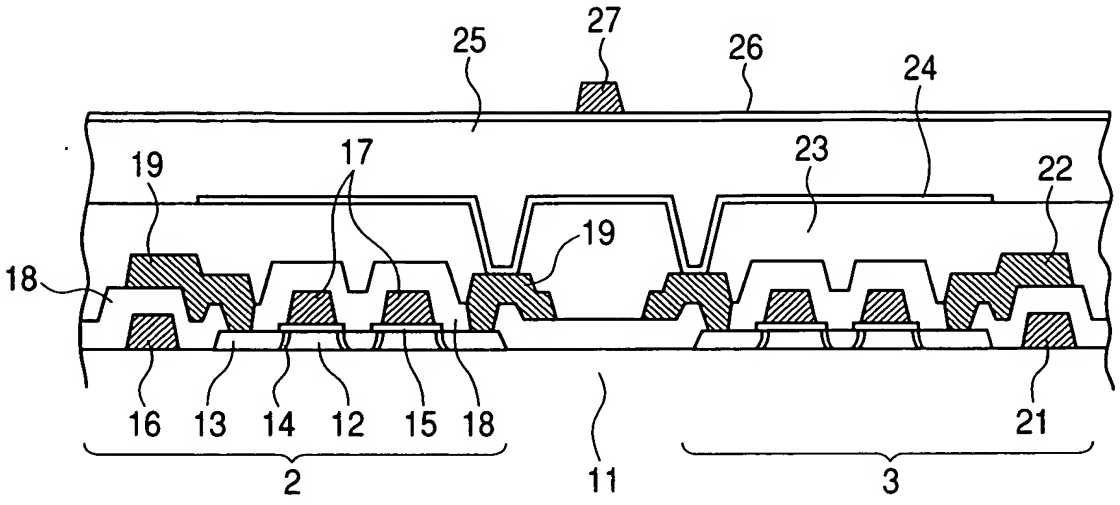

FIG. 4

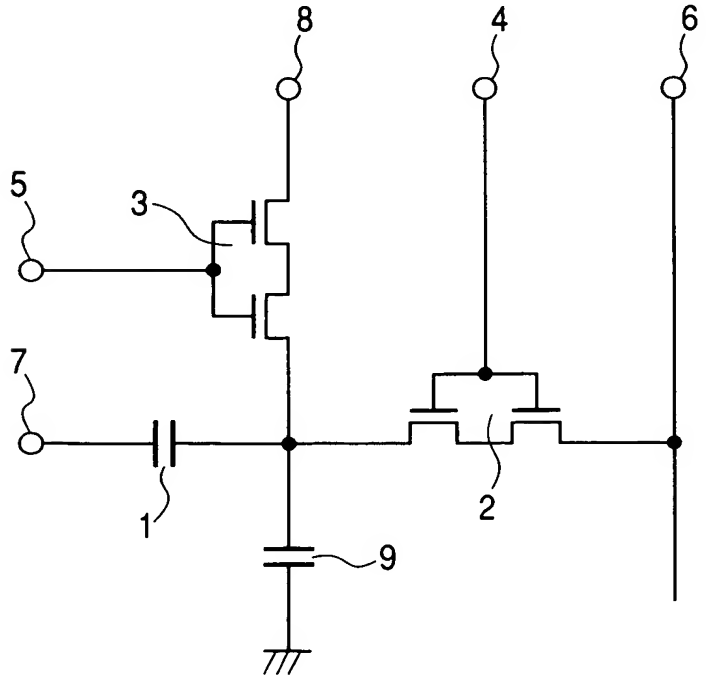

FIG. 5

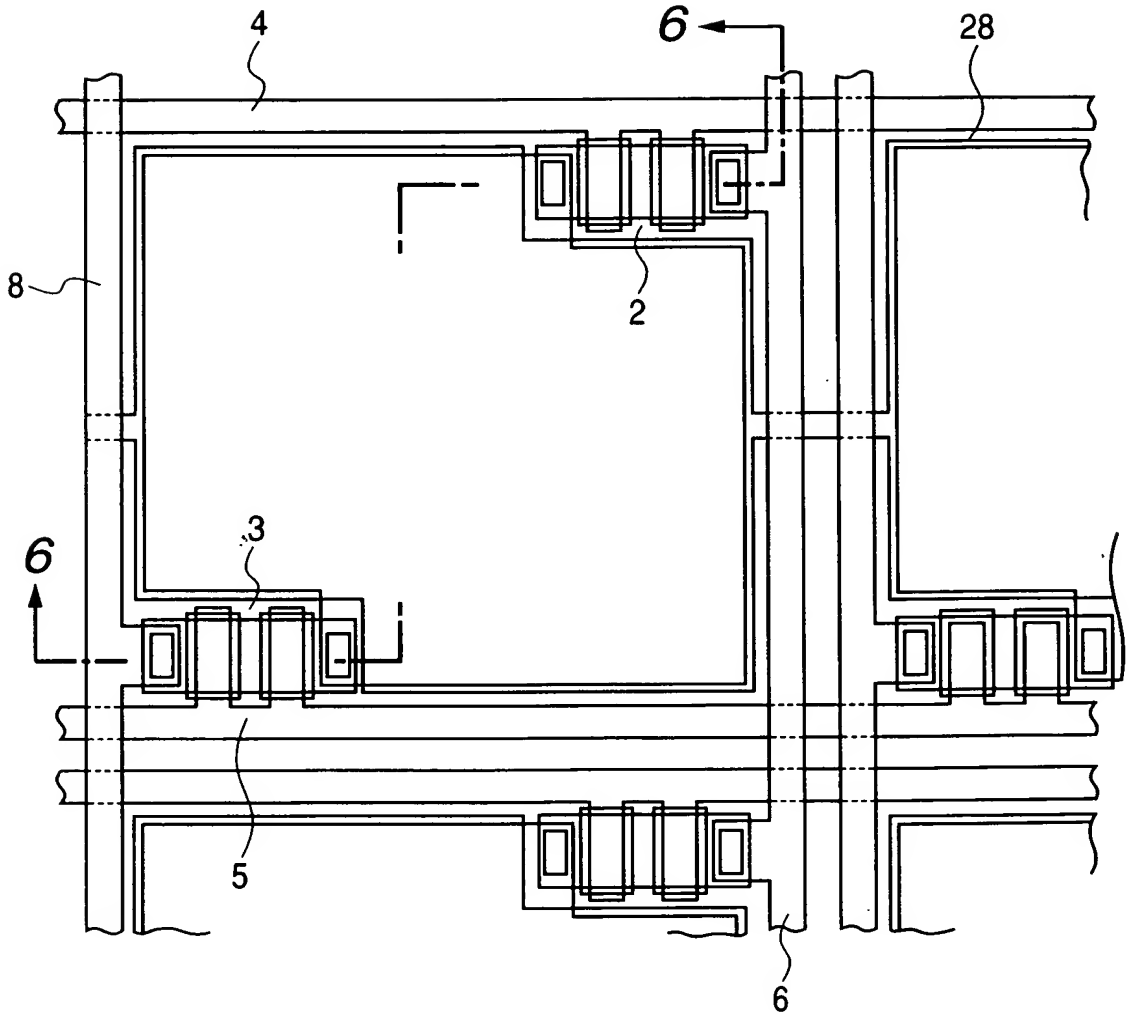

FIG. 6

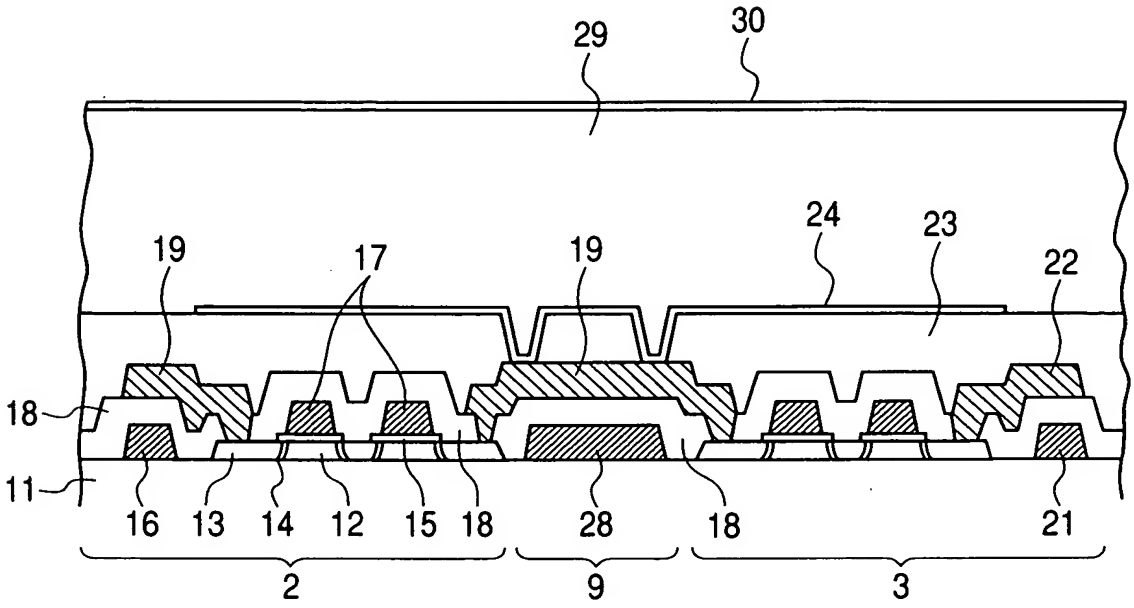
29
30
19
17
19
24
23
22
18
11
16
13
14
12
15
18
28
18
21
2
9
3

FIG. 7

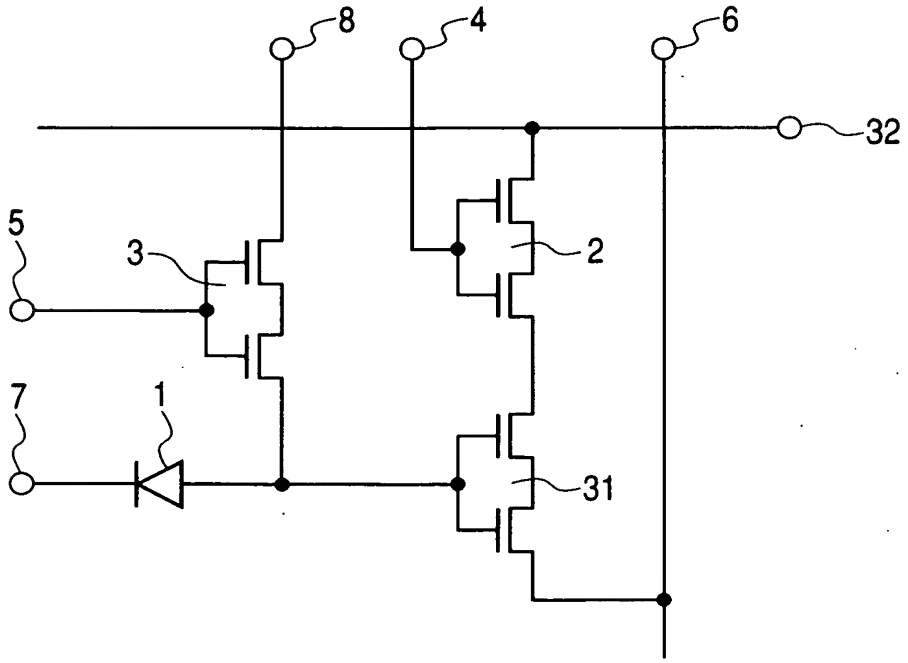
8
4
6
32
5
3
2
7
1
31

FIG. 8

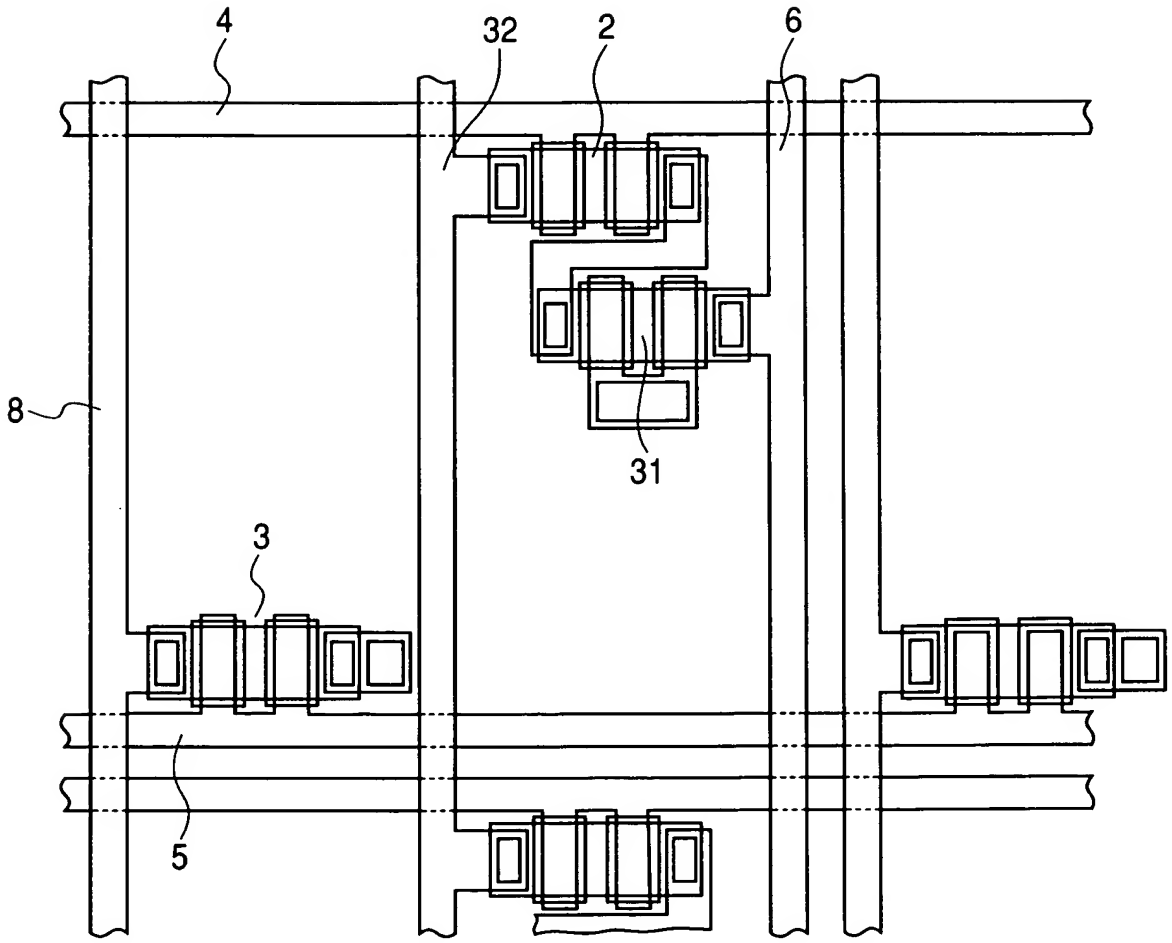

FIG. 9

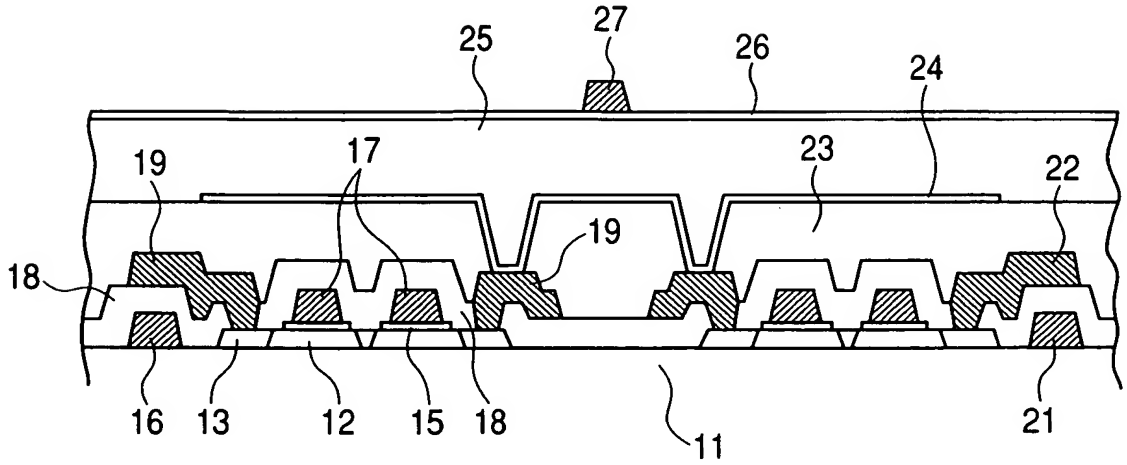

FIG. 10

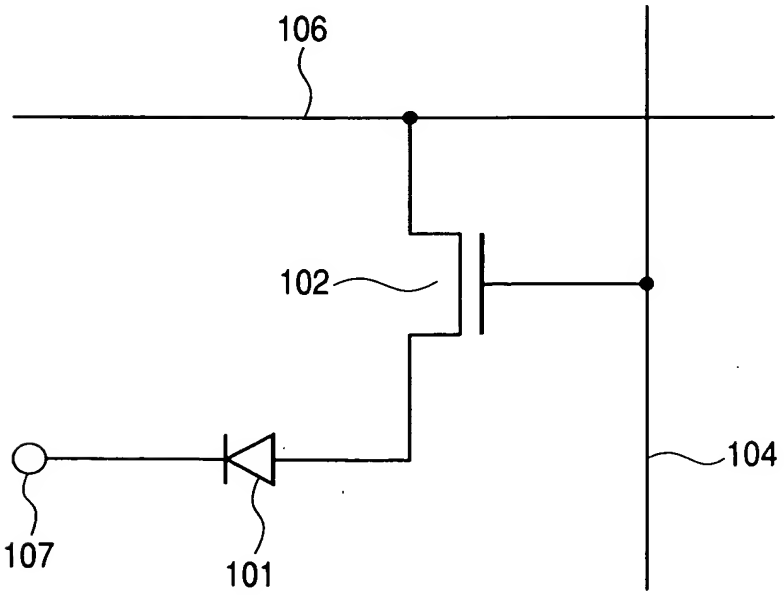

FIG. 11

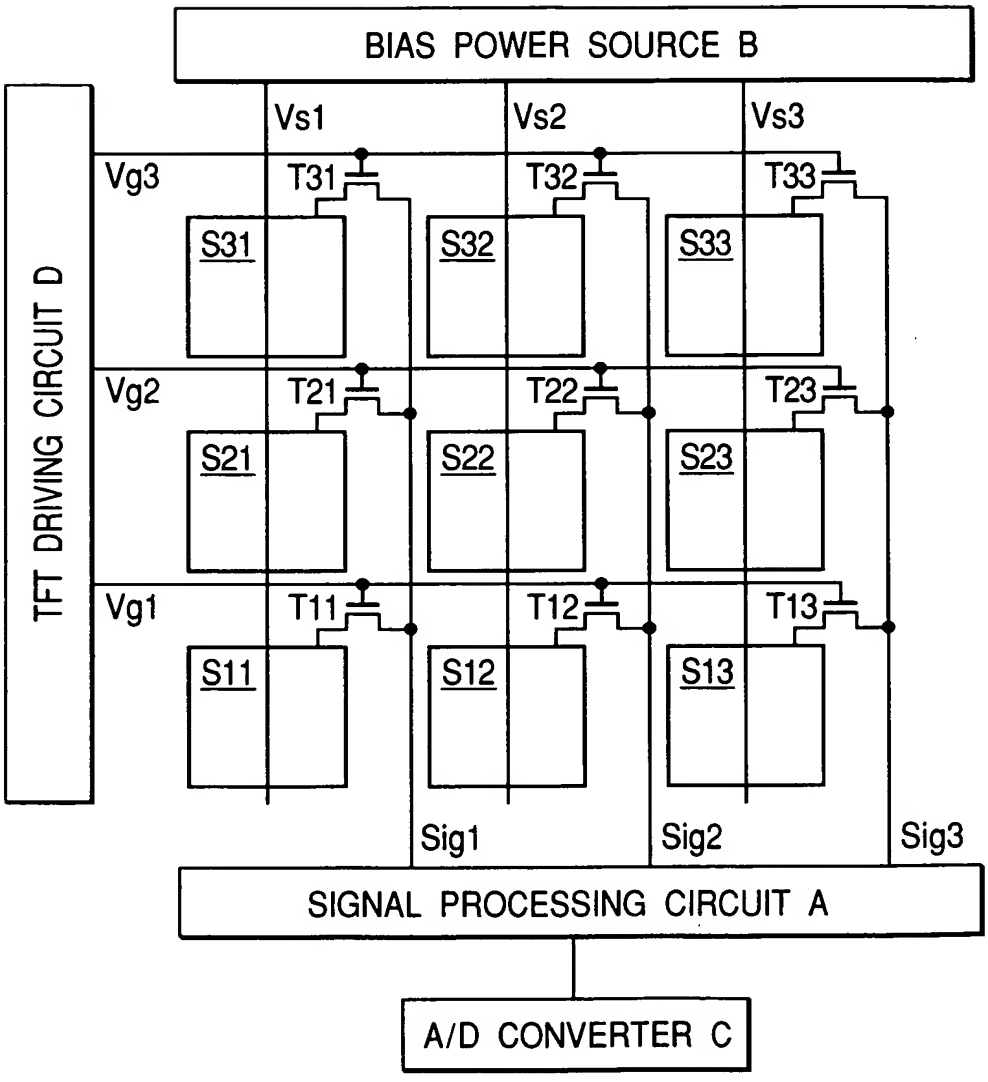
BIAS POWER SOURCE B
TFT DRIVING CIRCUIT D
Vs1
Vs2
Vs3
Vg3
Vg2
Vg1
T31
T32
T33
T21
T22
T23
T11
T12
T13
S31
S32
S33
S21
S22
S23
S11
S12
S13
Sig1
Sig2
Sig3
SIGNAL PROCESSING CIRCUIT A
A/D CONVERTER C

FIG. 12

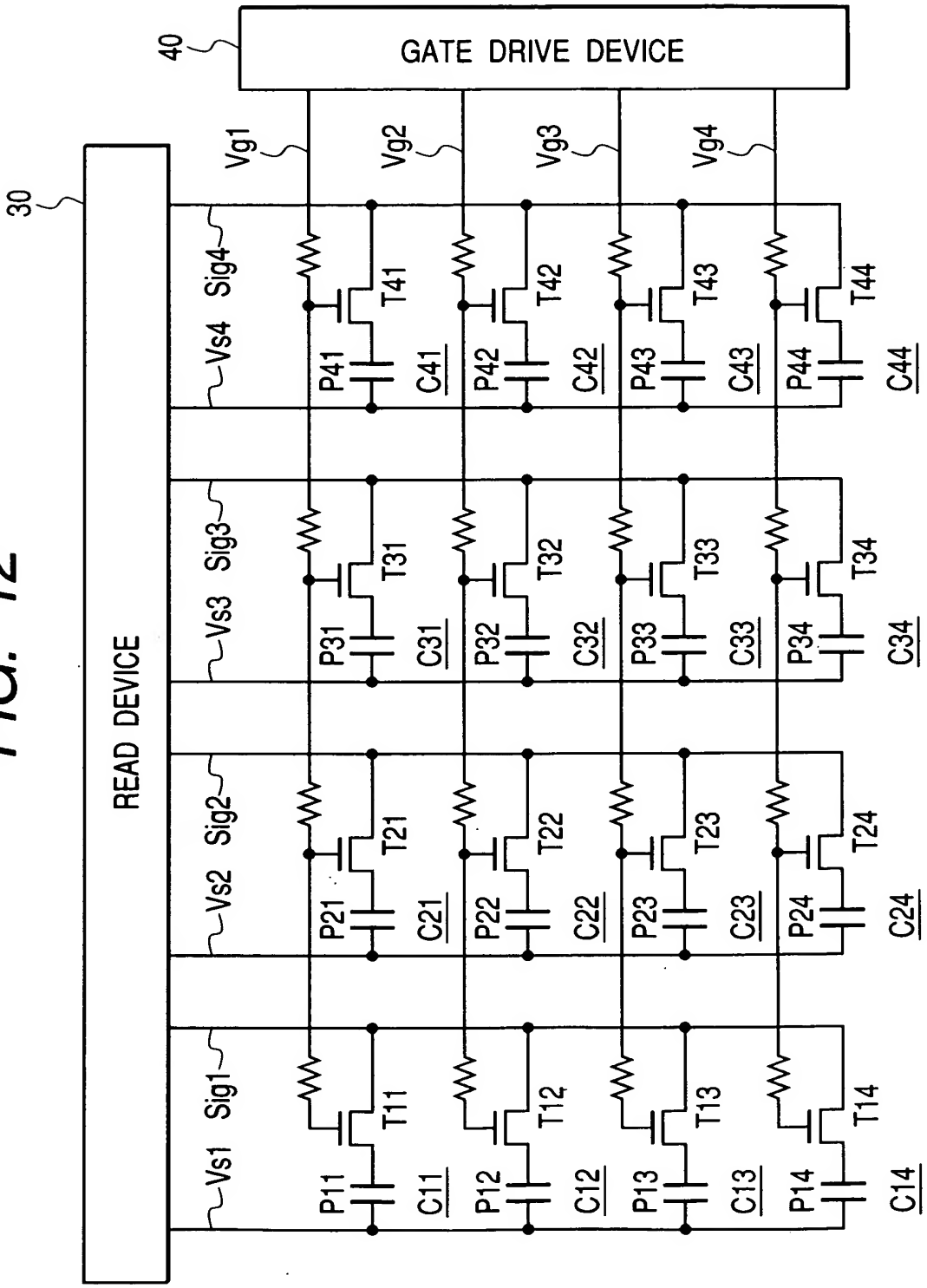
40
GATE DRIVE DEVICE
30
READ DEVICE
Vg1
Vg2
Vg3
Vg4
Vs1 Sig1
Vs2 Sig2
Vs3 Sig3
Vs4 Sig4
T11
T12
T13
T14
T21
T22
T23
T24
T31
T32
T33
T34
T41
T42
T43
T44
P11
P12
P13
P14
P21
P22
P23
P24
P31
P32
P33
P34
P41
P42
P43
P44
C11
C12
C13
C14
C21
C22
C23
C24
C31
C32
C33
C34
C41
C42
C43
C44

FIG. 13

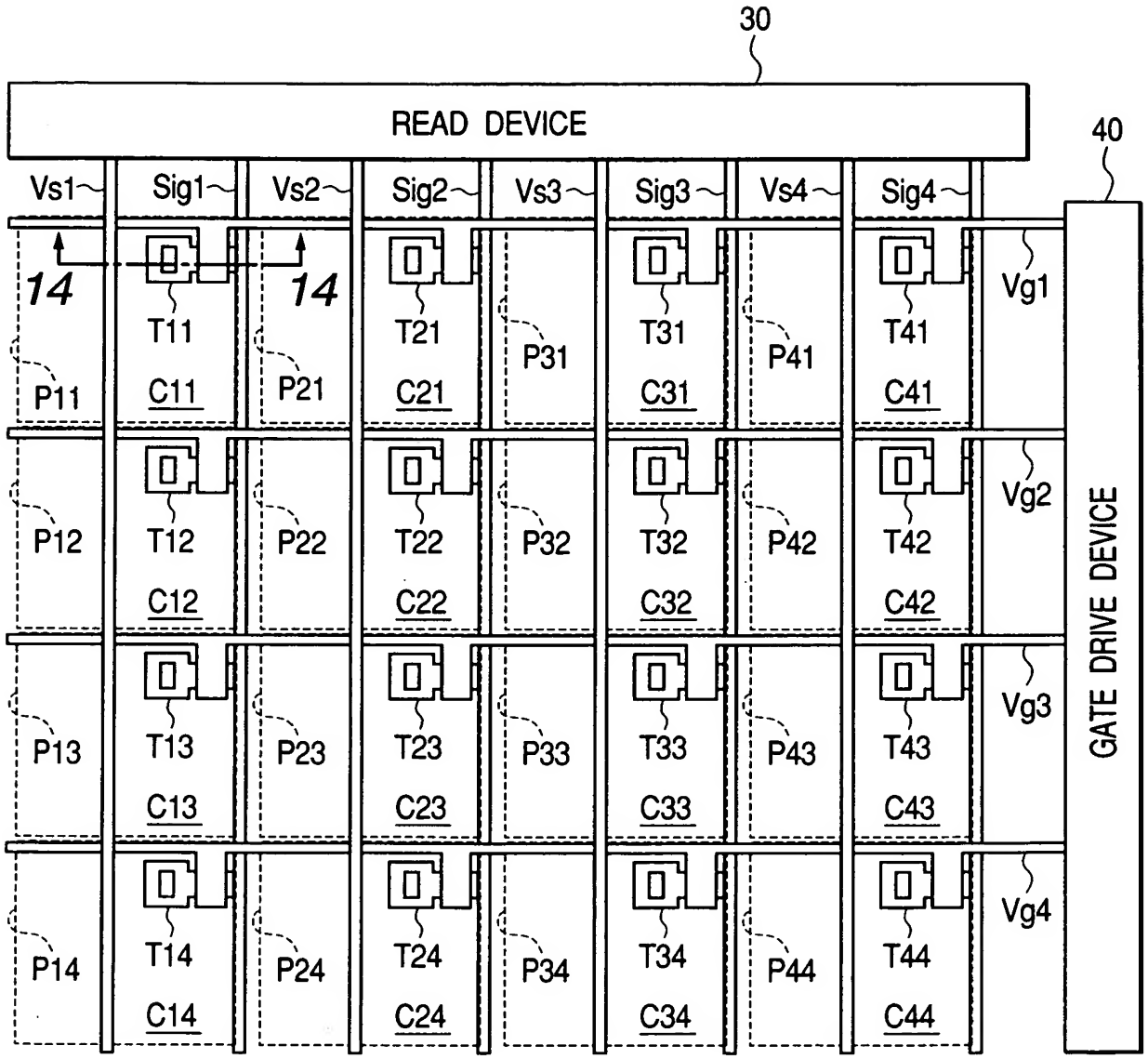
30
READ DEVICE
40
Vs1
Sig1
Vs2
Sig2
Vs3
Sig3
Vs4
Sig4
14
14
T11
C11
P11
P21
T21
C21
P31
T31
C31
P41
T41
C41
Vg1
P12
T12
C12
P22
T22
C22
P32
T32
C32
P42
T42
C42
Vg2
P13
T13
C13
P23
T23
C23
P33
T33
C33
P43
T43
C43
Vg3
P14
T14
C14
P24
T24
C24
P34
T34
C34
P44
T44
C44
Vg4
GATE DRIVE DEVICE

FIG. 14

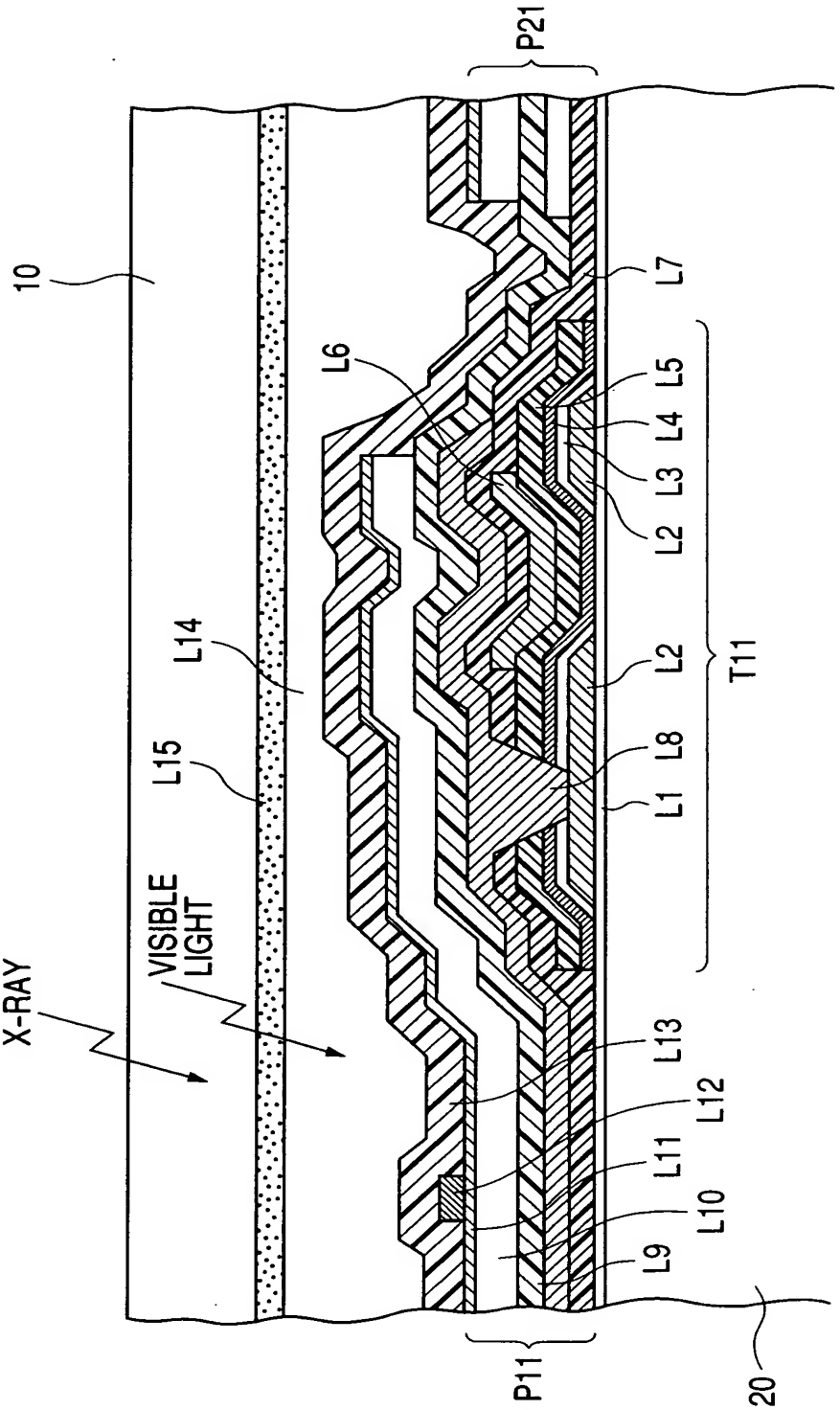
P21
10
L7
L6
L5
L4
L3
L2
L14
L2
T11
L15
L8
L1
VISIBLE LIGHT
X-RAY
L13
L12
L11
L10
L9
P11
20

FIG. 15

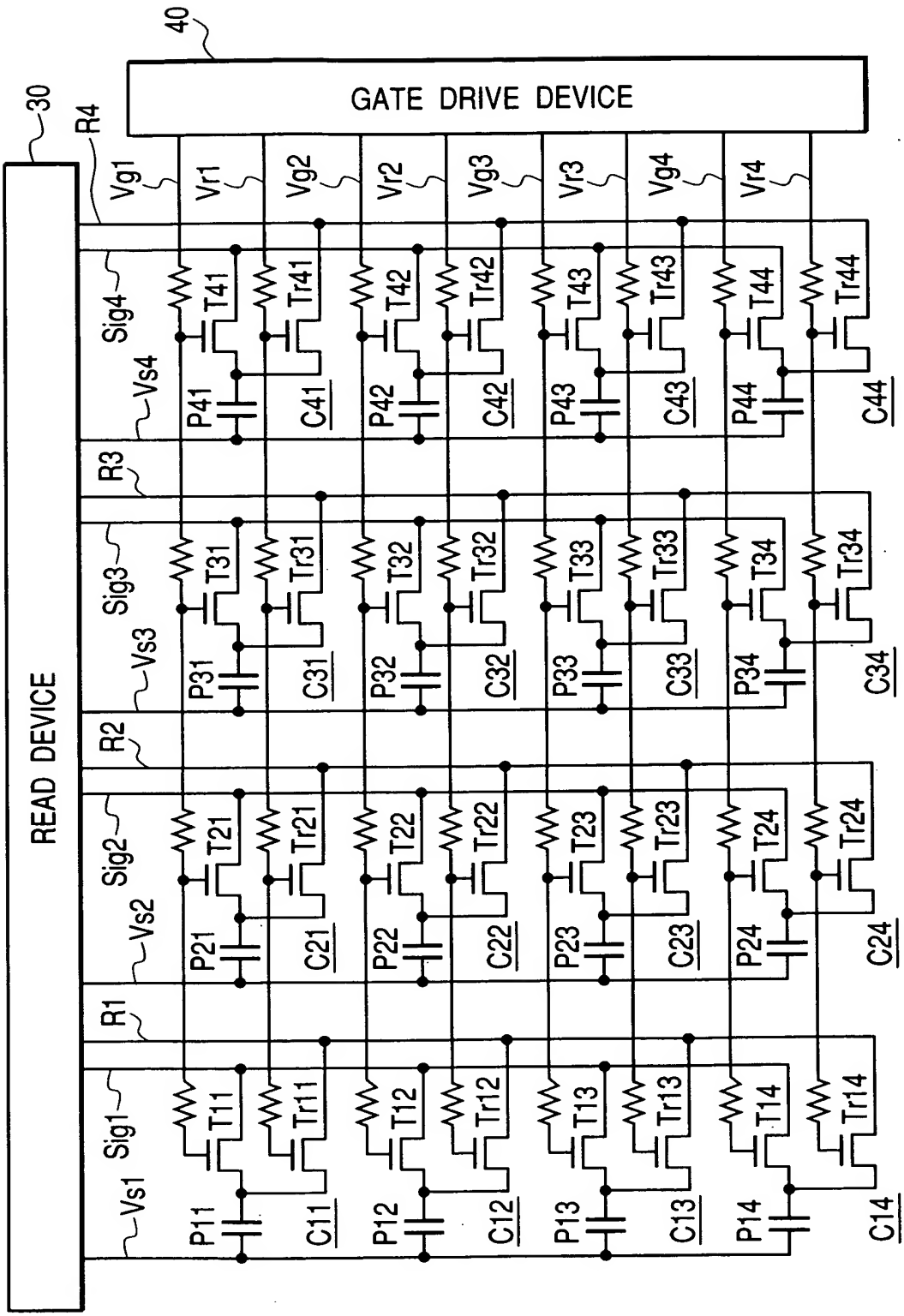
40
GATE DRIVE DEVICE
30
READ DEVICE
R4
R3
R2
R1
Vg1
Vr1
Vg2
Vr2
Vg3
Vr3
Vg4
Vr4
Sig4
Sig3
Sig2
Sig1
Vs4
Vs3
Vs2
Vs1
T41
Tr41
T42
Tr42
T43
Tr43
T44
Tr44
T31
Tr31
T32
Tr32
T33
Tr33
T34
Tr34
T21
Tr21
T22
Tr22
T23
Tr23
T24
Tr24
T11
Tr11
T12
Tr12
T13
Tr13
T14
Tr14
P41
C41
P42
C42
P43
C43
P44
C44
P31
C31
P32
C32
P33
C33
P34
C34
P21
C21
P22
C22
P23
C23
P24
C24
P11
C11
P12
C12
P13
C13
P14
C14

FIG. 16

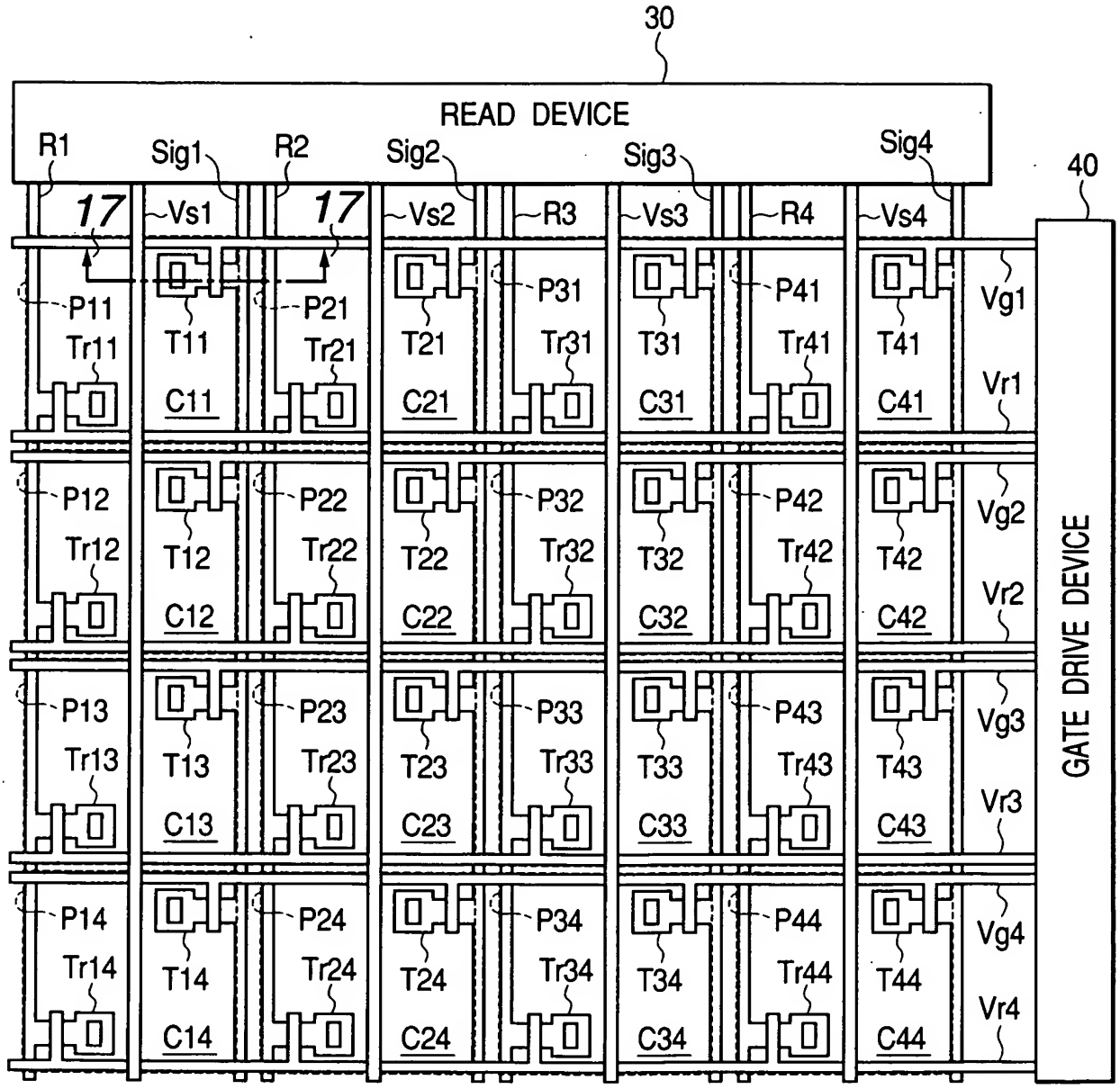
30
READ DEVICE
R1
Sig1
R2
Sig2
Sig3
Sig4
40
17
Vs1
17
Vs2
R3
Vs3
R4
Vs4
P11
Tr11
T11
C11
P21
Tr21
T21
C21
P31
Tr31
T31
C31
P41
Tr41
T41
C41
Vg1
Vr1
P12
Tr12
T12
C12
P22
Tr22
T22
C22
P32
Tr32
T32
C32
P42
Tr42
T42
C42
Vg2
Vr2
P13
Tr13
T13
C13
P23
Tr23
T23
C23
P33
Tr33
T33
C33
P43
Tr43
T43
C43
Vg3
Vr3
P14
Tr14
T14
C14
P24
Tr24
T24
C24
P34
Tr34
T34
C34
P44
Tr44
T44
C44
Vg4
Vr4
GATE DRIVE DEVICE

FIG. 17

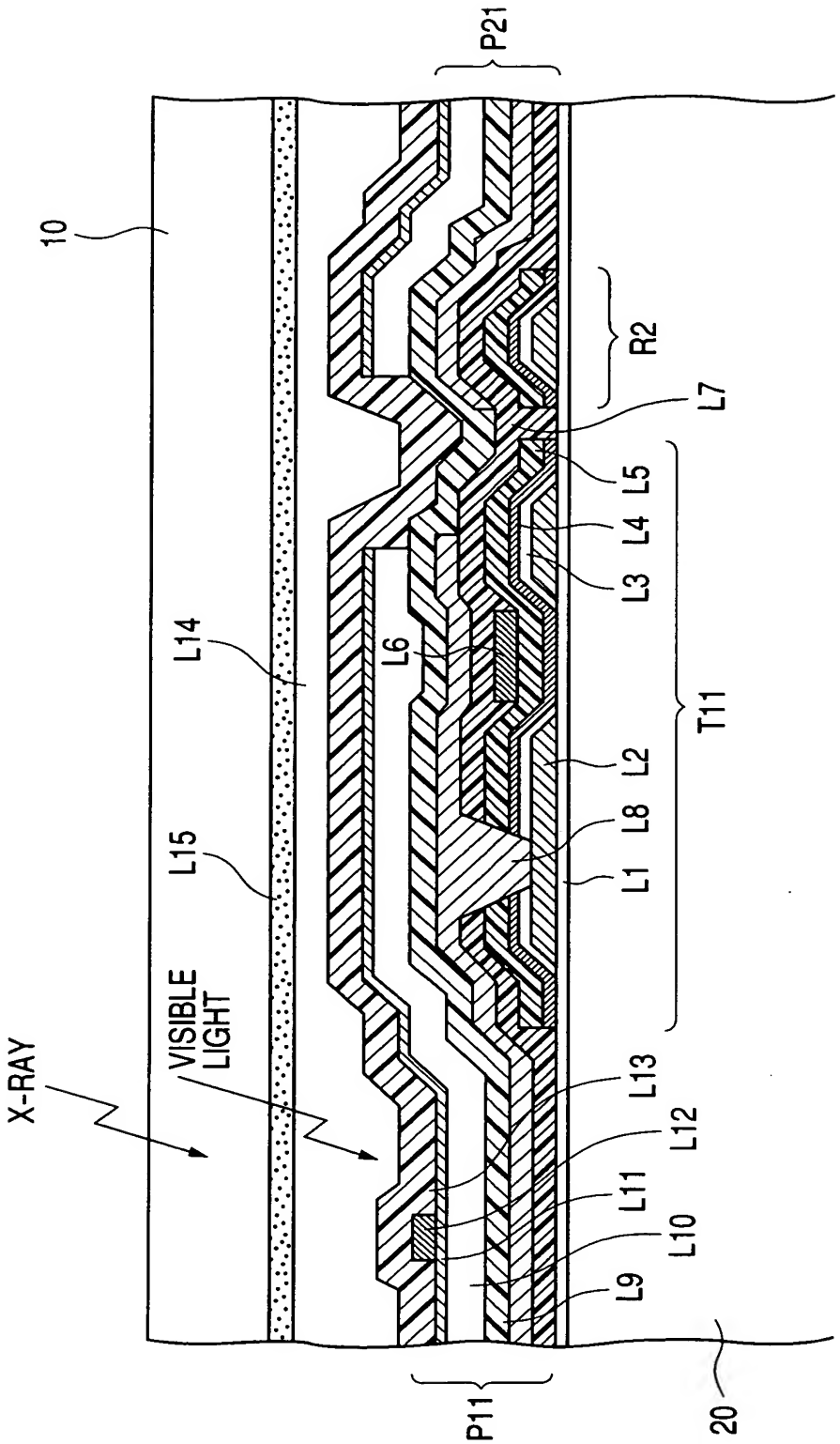
P21
10
R2
L7
L5
L4
L3
L14
L6
L2
T11
L8
L15
L1
VISIBLE LIGHT
X-RAY
L13
L12
L11
L10
L9
P11
20

FIG. 18

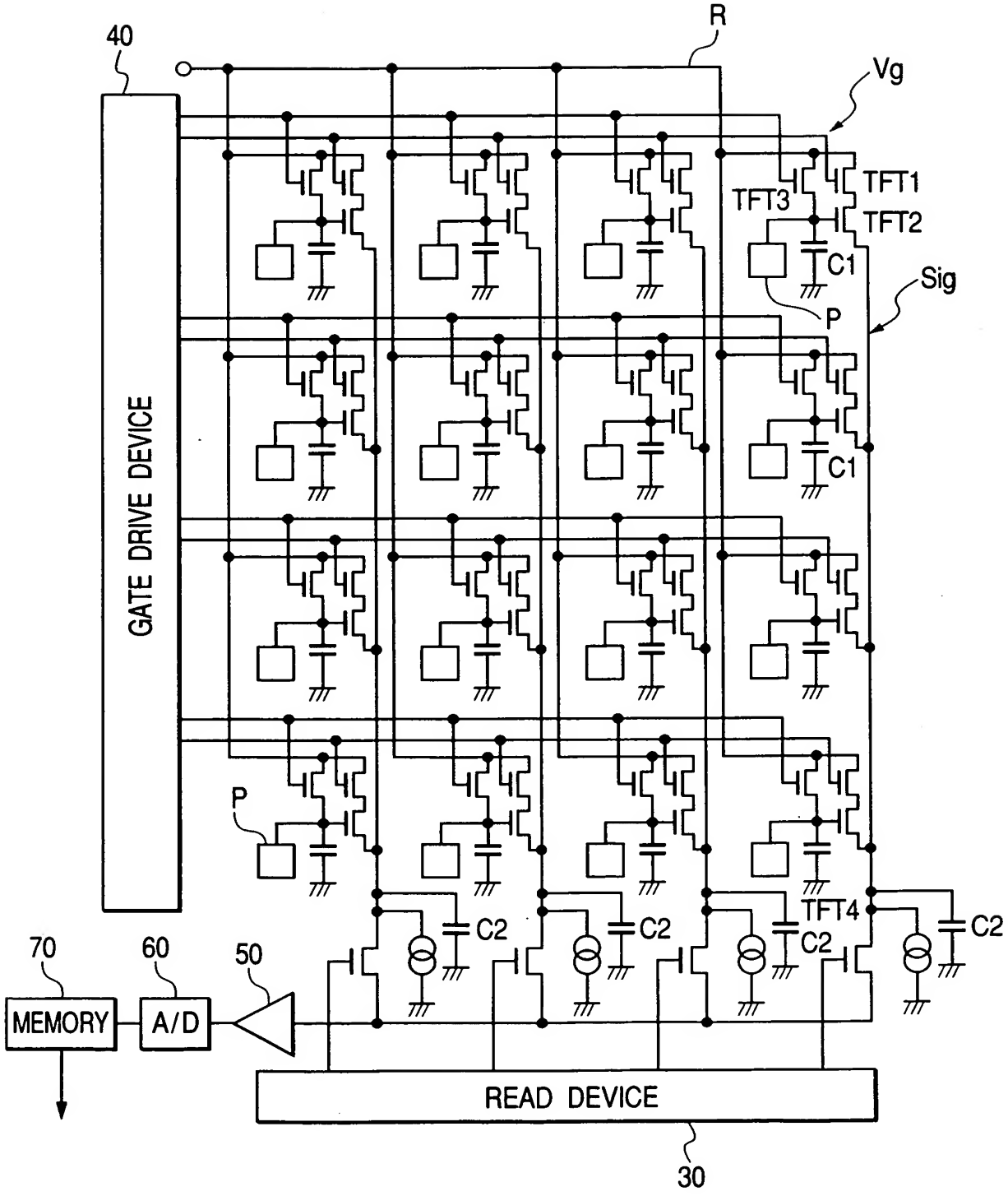
40
R
Vg
TFT1
TFT3
TFT2
C1
Sig
P
GATE DRIVE DEVICE
C1
P
TFT4
C2
C2
C2
C2
70
60
50
MEMORY
A/D
READ DEVICE
30

FIG. 19